

NCP1027ATXGEVB

A 5.0 V/2.0 A Standby Power Supply for Intel® Compliant ATX Applications Evaluation Board User's Manual



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EVAL BOARD USER'S MANUAL

ATX power supply units (PSU) require a standby section who keeps alive some particular areas of the motherboard. Among the live sections are the USB ports, the Ethernet controller and so on. The Intel ATX Power Supply Design Guide 2.01 (rev. June 04) describes the standby voltage rail needed for this purpose. This is the +5.0 VSB section (3.3.3):

- Output voltage: 5.0 V, $\pm 5\%$
- Nominal load current: 2.0 A
- 500 ms pulses current (USB wake-up event): 2.5 A
- Input power less than 1.0 W at 230 Vac for an output power of 500 mW
- Power on time: 2.0 s maximum
- Short circuit protection with auto-recovery

On top of these requirements, most of PSU designers use the standby power supply as an auxiliary rail to power the main controller. This is an auxiliary 12–13 V rail or, if an UC384X is implemented, this rail can go up to 20 V. When put in standby, a small switch shuts down the controller by interrupting this rail.

To help designers quickly fulfilling the above needs, the NCP1027 has been introduced. This DIP 8 package hosts a high performance controller together with a low $R_{DS(on)}$ 700 V BV_{dss} MOSFET. On top of the standby needs, we have packed other interesting goodies in this circuit. They are summarized below:

- **Brown-out detection:** the controller will not allow operation in low mains conditions. You can adjust the level at which the circuit starts or stops operation.
- **Ramp compensation:** designing in Continuous Conduction Mode helps to reduce conduction losses. However, at low input voltage (85 Vac), the duty-cycle might exceed 50%, and the risk exists to enter a subharmonic mode. A simple resistor to ground injects the right compensation level.
- **Over Power Protection:** a resistive network to the bulk reduces the peak current capability and accordingly harnesses the maximum power at high line. As this is

done independently from the auxiliary V_{CC}, the design gains in simplicity and execution speed.

- **Latch-off input:** some PC manufacturers require a complete latch-off in presence of an external event, e.g. overtemperature. The controller offers this possibility via a dedicated input.
- **Frequency dithering:** the switching frequency (here 65 kHz) is modulated during operation. This naturally spreads the harmonic content and reduces the peak value when analyzing the signature.



Figure 1. Evaluation Board Photo

Design Description

A full CCM operation gave us an adequate performance in this particular case, with good full load efficiency results as we will see. The part switches at 65 kHz which represents a good trade-off between switching losses and EMI control. A brown-out circuit was implemented, turning the SMPS on around 80 Vac and turning it off at 60 Vac. Different values can easily be selected by altering the dedicated resistive network. Please note that this network impedance has a direct influence on the standby power. To limit the amount of current the supply can deliver at high line, it is necessary to limit the propagation delay effects. The NCP1027 hosts an exclusive circuitry used to reduce the maximum peak current as the line increases. We will see that, once implemented around the auxiliary diode, it does not affect the standby power and nicely harnesses the maximum power. The electrical schematic of the board appears on Figure 2.

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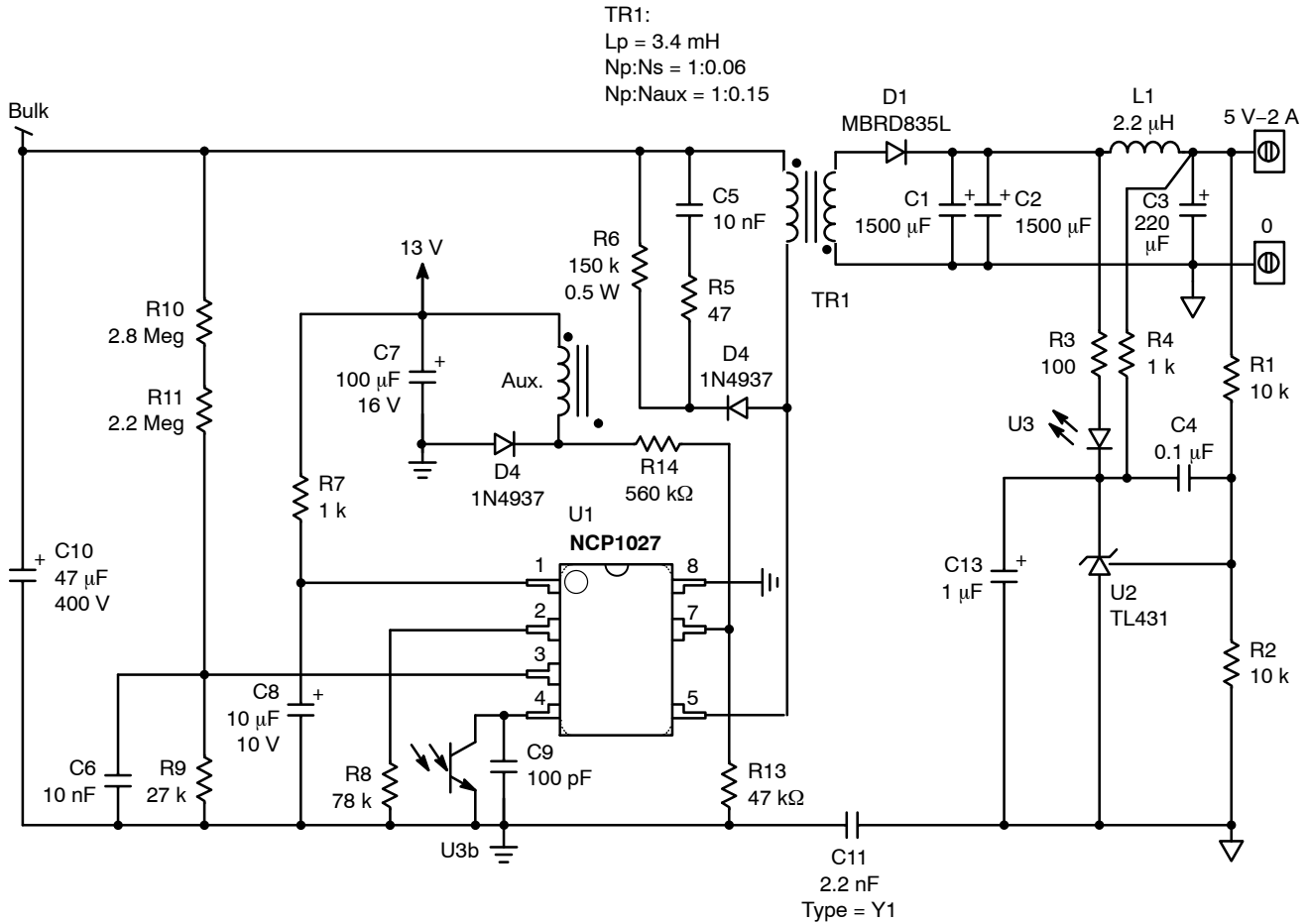


Figure 2. The Evaluation Board Electrical Schematic without the EMI Filter for Simpler Representation.

Let us start the review by the transformer description.

Transformer

The design of the transformer section represents the most difficult part as standby power in no-load and 0.5 W output must be respected. Various iterations have lead us to adopt the following characteristics:

$L_p = 3.4 \text{ mH}$

$N_p:N_s_{\text{power}} = 1:0.06$

$N_p:N_s_{\text{aux}} = 1:0.152$

The auxiliary winding in this case delivers 12.5 V but it can be set to any other value, depending on the main controller V_{CC} . The turn ratio limits the reflected value on the drain to less than 100 V, without risks of biasing the MOSFET body diode at the lowest input voltage. This transformer is available from Coilcraft under a reference detailed in the Bill Of Material (BOM).

As we have seen, our design operates in CCM at full load but obviously enters the Discontinuous Conduction Mode (DCM) at light loads. The transition point can be evaluated using the following formula:

$$R_c = 2L_p N^2 F_{sw} \left(\frac{NV_{in} + V_{out}}{NV_{in}} \right)^2 \quad (\text{eq. 1})$$

where:

L_p , the primary inductance, 3.4 mH

N , the turn ratio, 0.06

F_{sw} , the switching frequency, 65 kHz

V_{in} , the input voltage

V_{out} , the output voltage

Calculations lead to the following mode transition load values:

Lowest line, $V_{in} = 120 \text{ Vdc}$: $R_c = 4.56 \Omega$ or $I_{out} = 1.0 \text{ A}$

Highest line, $V_{in} = 370 \text{ Vdc}$: $R_c = 2.4 \Omega$ or $I_{out} = 2.0 \text{ A}$

Please note that low line is actually 85 Vac but the ATX PSU including a large bulk capacitor, we can neglect the ripple given the low output power of this converter, hence a 120 V value. At the highest line, the design operates at the boundary between CCM and DCM. The duty-cycle at full load and lowest input line can be evaluated via the flyback static transfer function:

$$D = \frac{V_{out}}{NV_{in} + V_{out}} \quad (\text{eq. 2})$$

The highest duty-cycle is found to be 41%. However, this number is likely to increase a little, given the presence of the leakage inductance.

Ramp Compensation

Being in CCM with a duty-cycle close to 50% (or above 50% in transient conditions), we need ramp compensation. Several ways exist to evaluate the amount of ramp compensation. The quickest one evaluates the *off* slope of the secondary inductance and injects around 50% of this slope through a compensating ramp (S_a) into the controller. With the NCP1027, the ramp compensation level is set via a simple resistor connected from pin 2 to the ground, as shown in Figure 2.

We can calculate the *off* slope, the one actually needed to evaluate S_a , by reflecting the output voltage over the primary inductance. The slope is projected over a complete switching period.

$$S_{off} = \frac{V_{out} + V_f}{N L_p} T_{sw} = \frac{6 \times 15 \mu}{0.06 \times 3.4 m} = 441 \text{ mA}/15 \mu s \quad (\text{eq. 3})$$

The NCP1027 features a current-mode architecture using a SENSEFET™ device. That is to say, the controller does not directly sense the current via a resistor but through a Kelvin cell. For this particular circuit, the cell ratio can be modeled as an equivalent sense resistor of 350 mΩ. This current slope will thus become a voltage slope having a value of:

$$S'_{off} = 0.441 \times 0.375 = 165 \text{ mV}/15 \mu s \quad (\text{eq. 4})$$

If we chose 50% of this down slope, then the final compensation ramp will present a slope of:

$$S_a = \frac{S'_{off}}{2} = 83 \text{ mV}/15 \mu s = 5.53 \text{ kV/s} \quad (\text{eq. 5})$$

Following the data sheet indications, we evaluate the resistor value to be:

$$R_{ramp} = \frac{7562}{0.083} = 91 \text{ k} \quad (\text{eq. 6})$$

In case no ramp compensation is required, pin 2 must be tied to V_{CC} , the adjacent pin. As experiments were carried at lower input voltages (C_{bulk} is small on the demo board), it was decided to slightly increase the amount of ramp compensation by reducing R_{ramp} to 78 kΩ.

Over Power Protection (OPP)

Power supply controllers sensing the primary current to check whether it goes over a certain limit often face propagation delay problems. That is to say, despite the current limit detection by a dedicated comparator, the information takes a certain amount of time to propagate through the logic circuits and eventually reset the latch. During this time, the primary current keeps increasing by a rate given by the primary inductance and the input voltage. Hence, we can quickly see the effects of a 100 ns delay at high line or low line:

$$I_{final} = I_{peak_max} + \frac{V_{in}}{L_p} t_{prop} \quad (\text{eq. 7})$$

If the limit is set to 750 mA, then we have:

$$I_{final} = 750 \text{ m} + \frac{100}{3.4 \text{ m}} 100 \text{ n} = 753 \text{ mA} \quad (\text{eq. 8})$$

$$I_{final} = 750 \text{ m} + \frac{374}{3.4 \text{ m}} 100 \text{ n} = 761 \text{ mA} \quad (\text{eq. 9})$$

The difference looks small but it often leads to a significant different in output current capabilities, especially with larger propagation delays. Hence, the need to act in high line conditions via a dedicated circuitry.

The NCP1027 hosts a special section used to reduce the maximum peak current limit as the mains increases. The system works by connecting a resistive network to the bulk capacitor, as Figure 3 depicts:

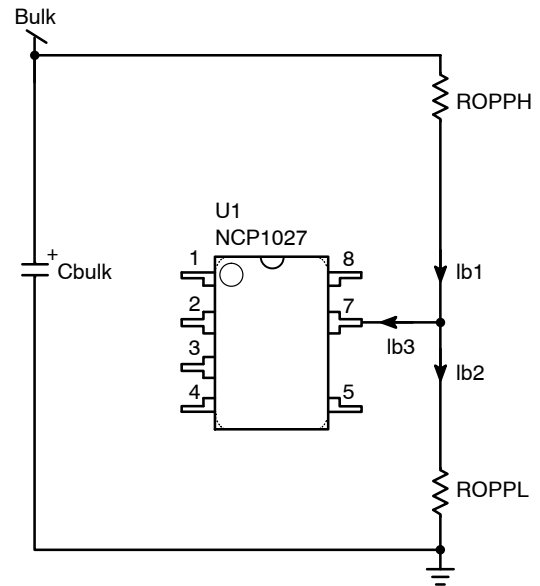


Figure 3. A Possible Option to Reduce the Peak Excursion consists of Connecting a Resistive Divider to the Bulk Capacitor.

By injecting a current I_{b3} proportional to V_{bulk} , the maximum peak current limits reduces. Analytically obtaining the right value for I_{b3} might represent a complicated exercise as many parameters play a role. To the opposite, a simple experimental method can be setup to obtain the value of the needed current:

1. Configure your working power supply as suggested by Figure 4 or 5. These figures are purposely simplified for ease of understanding of the added circuitry. Figure 4 represents the safest way to run the measurement as the dc power supply injects current via an optoisolator without sharing the converter's ground. An amp-meter is inserted to read the current I_{b3} . Leave the dc bias to zero for now.
2. Power the converter and set the input voltage to the highest of your specification. Let us assume it is 375 Vdc.

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3. Increase the output current to the point where the system should shut down per specification. Let's say 3.2 A for this design.
4. Start to increase the variable power supply dc voltage until the amp-meter deviates. Increase carefully because you deal with hundred of μA only.
5. At a certain time, if you continue to increase the current in pin 7, the converter enters in protection mode. The current flowing in pin 7 and the voltage on it prior to the shutdown, correspond to the variables you look for. In this example, we measured a V_f voltage of 2.45 V and a current of 31 μA .

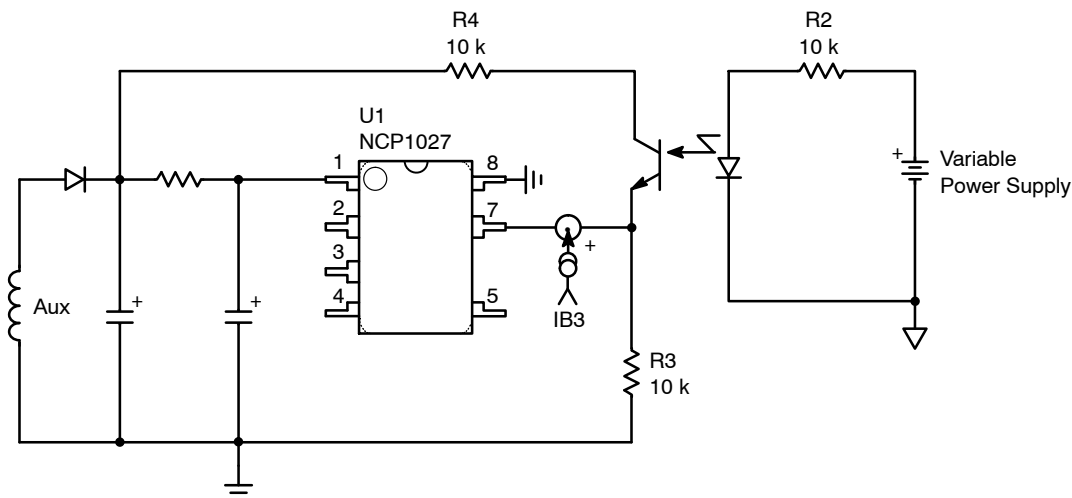


Figure 4. An Isolated Way to safely Inject Current into Pin 7 at High Line.

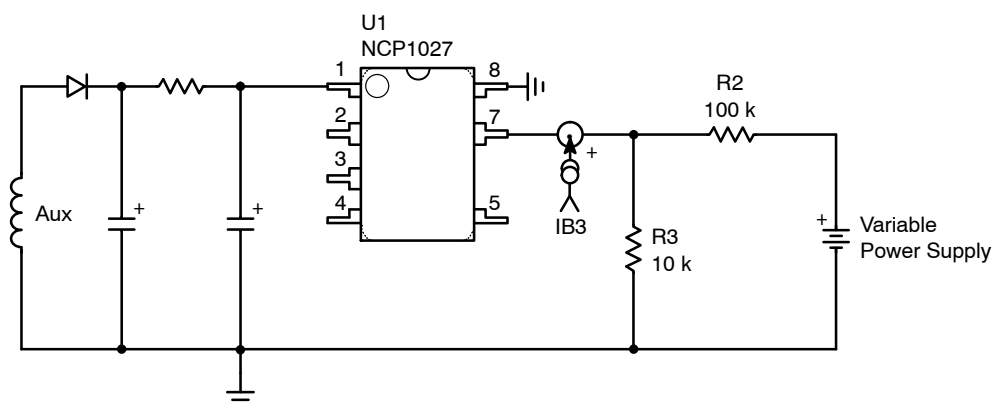


Figure 5. A Non-isolated Way to Inject Current into Pin 7 at High Line.

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The preliminary curve showing the relationship between the injected current and the maximum peak current setpoint appears in Figure 6. We can see that 31 μA corresponds to

a 20% reduction in the maximum peak current capability. The V_f parameter specifies the voltage at which pin 7 starts to pump in current. It is around 2.5 V as we can see it.

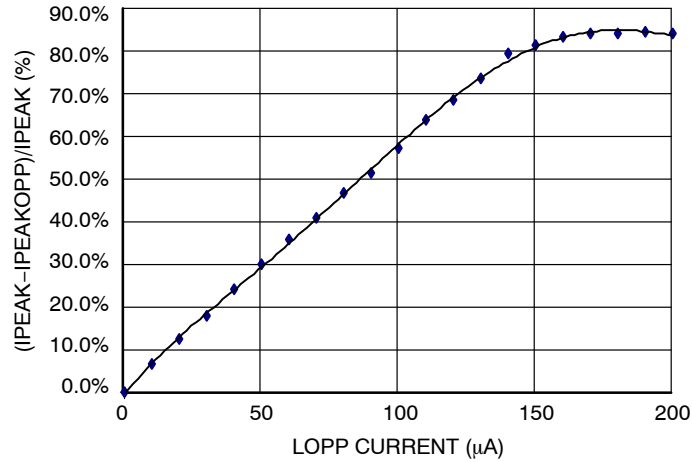


Figure 6. Maximum Peak Current Setpoint Reduction vs. Pin 7 Injected Current

To compute the resistor values, we need to define the range within which the OPP reduction should activate. As we do not want any OPP action at low input voltages, we will select resistors to start reducing at $V_{in} = 200 \text{ Vdc}$, with a clamp at $V_{in} = 375 \text{ Vdc}$. Using the following equations and our collected data leads us to the final values:

$$\begin{aligned} V_{bulkH} &= 375 \text{ Vdc} \\ V_{bulkL} &= 200 \text{ Vdc} \\ I_{OPP} &= 31 \mu\text{A} \\ V_f &= 2.45 \text{ V} \end{aligned}$$

$$R_{OPPL} = \frac{V_{bulkH} - V_{bulkL}}{I_{OPP}(V_{bulkL} - V_f)} V_f = 70 \text{ k}\Omega \quad (\text{eq. 10})$$

$$R_{OPPH} = R_{OPPL} \frac{V_{bulkL} - V_f}{V_f} = 5.6 \text{ M}\Omega \quad (\text{eq. 11})$$

Unfortunately, despite the good behavior of the network, its permanent presence on the bulk rail will affect the consumption in standby. When you chase every hidden milli-watt, it can become a nasty problem. To avoid this trouble, a simple solution around the auxiliary winding can be worked out. This is presented in Figure 7. During the on time, where the power switch is turned on, the input voltage appears across the primary transformer. Given the auxiliary diode configuration, $N \cdot V_{in} + V_{out}$ also appears on the cathode, N being the primary to secondary turn ratio. As this voltage moves up and down with the bulk level, we can perfectly use it for our OPP purposes. Due to its pulsating low voltage nature, power consumption will be the smallest.

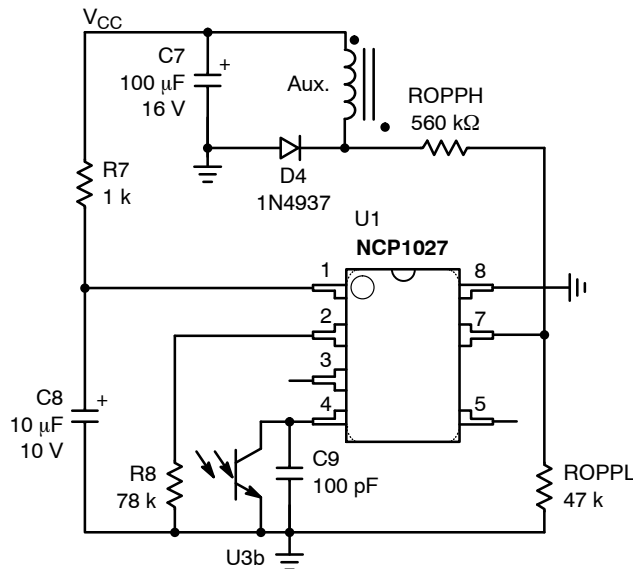


Figure 7. The Auxiliary Diode lends itself very well to a cheap and energy efficient OPP Implementation.

Hooking an oscilloscope probe on D_4 cathode gives us the bulk image evolution between its minimum and maximum values. We can then run the calculation again to obtain R_{OPPH} and R_{OPPL} :

$$\begin{aligned} V_{bulkH} &= 55 \text{ Vdc} \\ V_{bulkL} &= 37 \text{ Vdc} \\ I_{OPP} &= 31 \mu\text{A} \\ V_f &= 2.45 \text{ V} \end{aligned}$$

$$\begin{aligned} R_{OPPH} &= 580 \text{ k}\Omega \rightarrow 560 \text{ k}\Omega \text{ after tweak} \\ R_{OPPL} &= 41 \text{ k}\Omega \rightarrow 47 \text{ k}\Omega \text{ after tweak} \end{aligned}$$

Figure 8 shows the results before and after OPP implementation. The output current stays below 3.5 A in all cases which is well within specs.

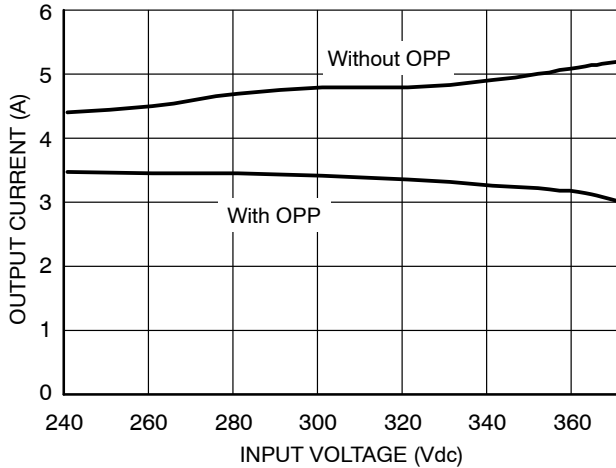


Figure 8. Over Power Protection at work keeps the output current below 3.5 A.

Brown-out

Brown-out (BO) detection offers a means to protect the converter in presence of low input voltages by stopping switching operation until the mains comes back to a normal value. The circuit works by observing a fraction of the bulk level via a resistive divider routed to pin 2. When the level on pin 2 lies below 0.6 V, the controller does not allow switching operation, but the high-voltage current source maintains the V_{CC} on pin 1. Then, as soon as pin 2 voltage crosses 0.6 V, the V_{CC} is ready to power the chip and switching can start. As this occurs, pin 2 injects around 12 μA (I_{BO}) in the resistive bridge to create a hysteresis. The designer must thus select the turn-on and turn-off voltages to further apply the following equations:

$$R_{upper} = R_{lower} \frac{V_{bulk1} - V_{BO}}{V_{BO}} \quad (\text{eq. 12})$$

$$R_{lower} = V_{BO} \frac{V_{bulk1} - V_{bulk2}}{I_{BO} \times (V_{bulk1} - V_{BO})} \quad (\text{eq. 13})$$

Suppose we want to start at $V_{in} = 110 \text{ Vdc}$ (77 Vac) and stop operation at $V_{in} = 70 \text{ Vdc}$ (50 Vac), then applying Equations 12 and 13 leads to the following values:

$$\begin{aligned} R_{upper} &= 4.0 \text{ M}\Omega \\ R_{lower} &= 22 \text{ k}\Omega \end{aligned}$$

Total power dissipation at nominal line is then

$$P_{BO} = \frac{3302}{4.02 \text{ Meg}} = 27 \text{ mW.}$$

On the board, we purposely modified these values to further improve the standby power.

Auxiliary Winding

The auxiliary winding is set to deliver 13 V nominal when the converter is fully loaded. To avoid any V_{CC} drops during transient loading, e.g. sudden load removal, the main V_{CC} capacitor C_7 has been increased to 100 μF , leading to a stable V_{CC} in no-load conditions. The resistor R_7 sets the Overvoltage Protection (OVP) level by adjusting the injected current in pin 1 internal shunt in case of problems. With 1.0 k Ω , the OVP level is set to $V_{OVP} = 1.0 \text{ k} \cdot 7.0 \text{ m} + 8.7 = 15.7 \text{ V}$ typical on the auxiliary winding. Different values can be obtained by changing the resistor values or the ratio between the power and auxiliary windings.

Clamping Section

The converter uses an RCD clamp to safely limit the voltage excursion on the MOSFET drain. Failure to keep $V_{ds}(t)$ below 700 V will permanently damage the circuit. In application where the input line can be subject to strong high-voltage parasitic pulses, we recommend the usage of a Transient Voltage Suppressor (TVS), that will hard clamp all potentially lethal spikes on the drain. Figure 9 portrays the way to wire the TVS. Finally, the TVS offers superior performance in standby power compared to the RCD clamp. Simply because the RCD clamp always activates since the capacitor discharges via the resistor R as soon the leakage inductance is reset. Unfortunately, even in standby, this mechanism generates light losses. If you want to further save 50 mW, a TVS is of good usage. A 200 V TVS has shown to be a good solution here. You can use the 1.5KE200A from ON Semiconductor for instance.

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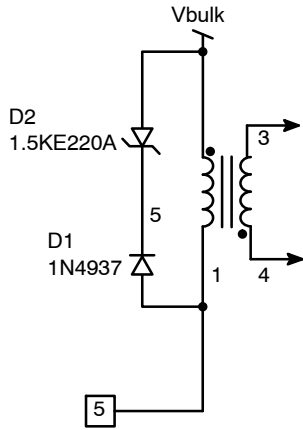


Figure 9. A TVS must be used if the Input Voltage can be subject to High Voltage Spikes.

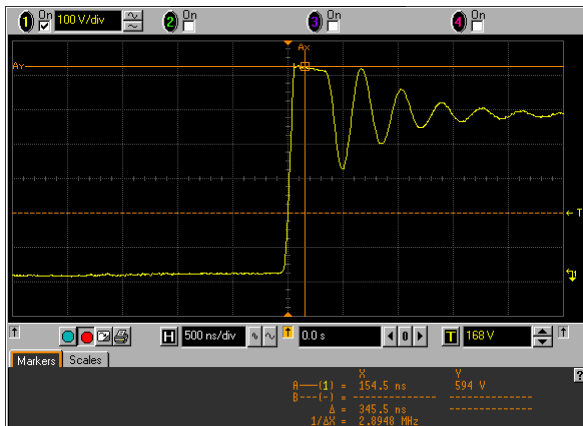


Figure 10. Always Check the Voltage on the Drain at the highest Line Condition (265 Vac).

Secondary Side

The secondary side uses a Schottky diode featuring an 8.0 A capability and a breakdown voltage of 35 V. This is enough since high line conditions imply a Peak Inverse Voltage (PIV) of:

$$\text{PIV} = NV_{\text{in}} + V_{\text{out}} = 0.06 \times 370 + 5 = 27.2 \text{ V} \quad (\text{eq. 14})$$

The forward voltage V_f goes down to 0.41 V @ $T_j = 125^\circ$ which, neglecting ohmic losses, induces conduction losses of:

$$P_{\text{diode}} = I_{\text{RMS}}^2 R_d + I_{\text{avg}} V_f \approx 2 \times 0.41 = 0.8 \text{ W} \quad (\text{eq. 15})$$

The output capacitor C_{out} is selected to a) pass the adequate RMS current b) limit the undershoot ΔV when the output is banded by a current step ΔI . The undershoot depth of a closed-loop converter having a bandwidth f_c can be evaluated via the following formula:

$$\Delta V = \frac{\Delta I}{f_c C_{out}} \quad (\text{eq. 16})$$

Calculations gave us a value of 2.4 mF, made of two low-impedance 10 V/1200 μ F capacitors.

A TL431 ensures a stable regulation at 5.0 V via a type-2 amplifier. R_3 and the NCP1027 internal pullup resistor set the midband gain, whereas C_4 sets the zero position. The small capacitor C_9 filters out residual noise and adds a high frequency pole, acting together with the optocoupler one. The step load response is clean, without any ringing at both high and low line conditions. The circuit can be slightly modified to add some more soft-start, in case designers would fear output overshoots. Figure 11 shows how to connect a 1.0 $\mu\text{F}/10\text{ V}$ capacitor to soften the start-up sequence:

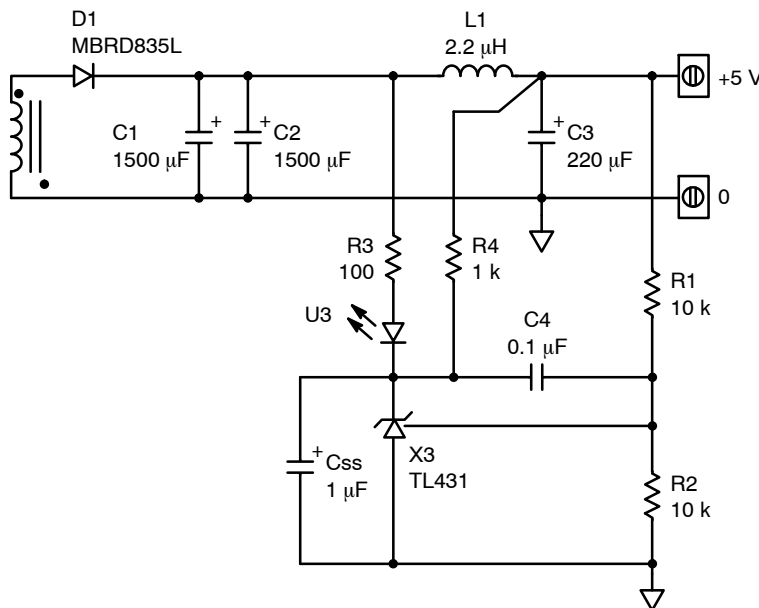


Figure 11. A 1.0 μ F Capacitor connected on the TL431 strengthens the Startup Sequence.

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The basic description being done, let us have a look at the board performance. Standby measurements were captured with a Yokogawa WT210 on a board after it warmed up for 15 minutes. Please make sure the WT210 volt-meter is placed before the current shunt, otherwise its input impedance will degrade the low-power measurements by 30 mW at high line.

Static Measurements

$V_{in} = 230 \text{ Vac}$
 $T_{ambient} = 25^{\circ}\text{C}$

$P_{out} = 0$	$P_{in} = 88 \text{ mW}$	$V_{aux} = 10.14 \text{ V}$	
$P_{out} = 0.5 \text{ W}$	$P_{in} = 779 \text{ mW}$	$V_{aux} = 11.64 \text{ V}$	$\eta = 64.2\%$
$P_{out} = 10 \text{ W}$	$P_{in} = 12.3 \text{ W}$	$V_{aux} = 12.14 \text{ V}$	$\eta = 81.3\%$

→ Please note that replacing R_6 by a 200 V TVS as mentioned in the text, reduces the input power at 0.5 W @ 230 Vac down to 715 mW and 73 mW at no load.

$P_{out} = 0$	$P_{in} = 98 \text{ mW}$ at $V_{in} = 265 \text{ Vac}$ with RCD
$P_{out} = 0$	$P_{in} = 85 \text{ mW}$ at $V_{in} = 265 \text{ Vac}$ with TVS

$T_{case} \text{ NCP1027} = 50^{\circ}\text{C}$ at $P_{out} = 10 \text{ W}$

Short-circuit temperature: $T_{case} \text{ NCP1027} = 42^{\circ}\text{C}$, $T_{diode} = 52^{\circ}\text{C}$
Maximum output current: 3.0 A @ 265 Vac

$V_{in} = 85 \text{ Vac}$
 $T_{ambient} = 25^{\circ}\text{C}$

$P_{out} = 0$	$P_{in} = 54 \text{ mW}$	$V_{aux} = 10.15 \text{ V}$	
$P_{out} = 0.5 \text{ W}$	$P_{in} = 704 \text{ mW}$	$V_{aux} = 11.6 \text{ V}$	$\eta = 71\%$
$P_{out} = 10 \text{ W}$	$P_{in} = 12.6 \text{ W}$	$V_{aux} = 12.6 \text{ V}$	$\eta = 79.5\%$

$T_{case} \text{ NCP1027} = 60^{\circ}\text{C}$ at $P_{out} = 10 \text{ W}$

Short-circuit temperature: $T_{case} \text{ NCP1027} = 44^{\circ}\text{C}$, $T_{diode} = 52^{\circ}\text{C}$
Maximum output current: 3.1 A

Dynamic Measurements

Some critical waveforms have been captured on the demonstration board and are reproduced below:

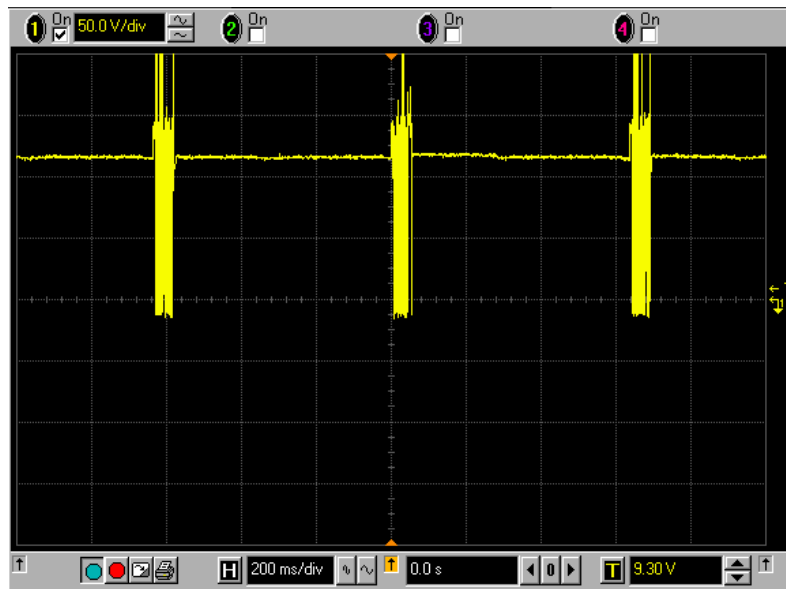


Figure 12. Short-Circuit Protection, Drain-Source Waveform

In Figure 12, we can see the power supply operating in a so-called hiccup mode, trying to re-start as soon as the internal timer has elapsed. The resulting duty-burst stays

below 8%, keeping all component temperatures at a moderate level. This is an auto-recovery type of protection, implying a re-start when the fault is removed ($V_{in} = 230 \text{ Vac}$).

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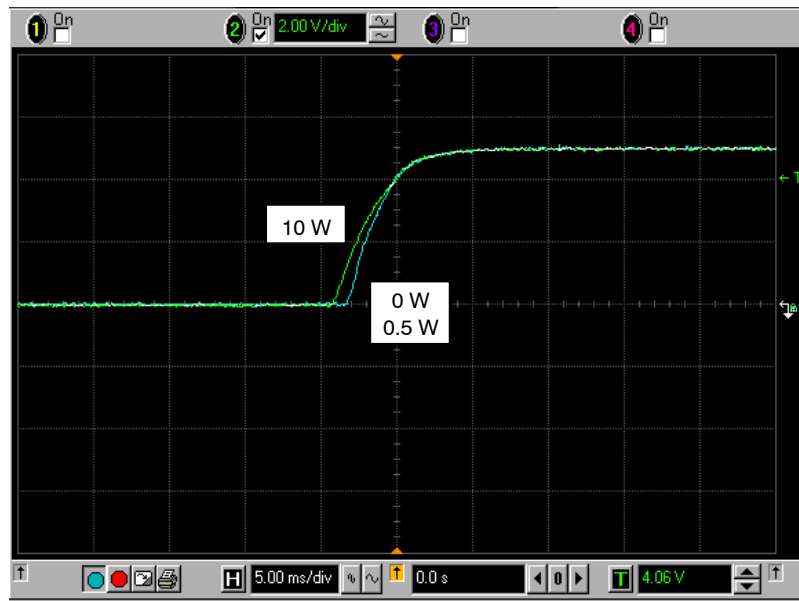


Figure 13. Startup Sequence at Three Loading Conditions

Figure 13 shows a typical startup sequence, captured at different output levels (0, 0.5 W and 10 W) for $V_{in} = 85 \text{ Vac}$. Changing the input voltage does not modify the shape of the

waveform. This waveform has been captured with the 1.0 μF wired as suggested by Figure 11.

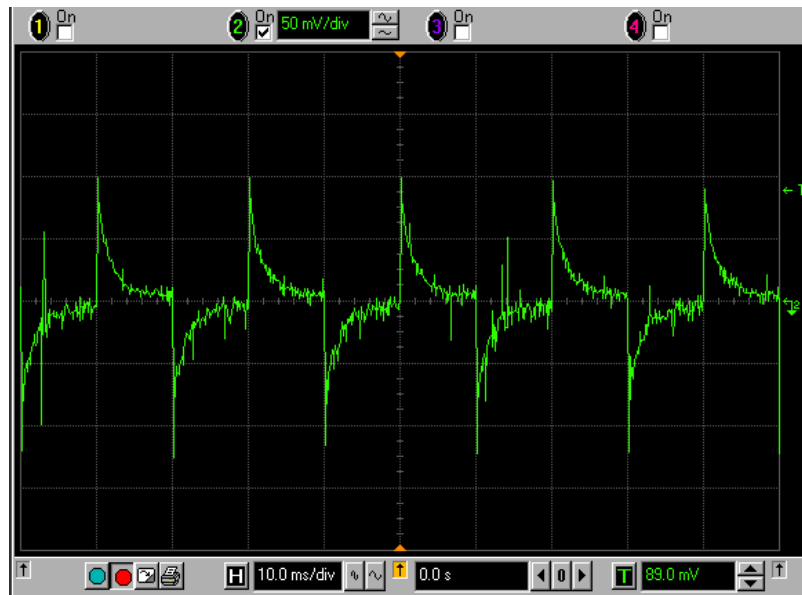


Figure 14. Load step where V_{out} is banded from 0.1 A to 2.5 A with a 1.0 A/ μs slew-rate ($V_{in} = 85 \text{ Vac}$).

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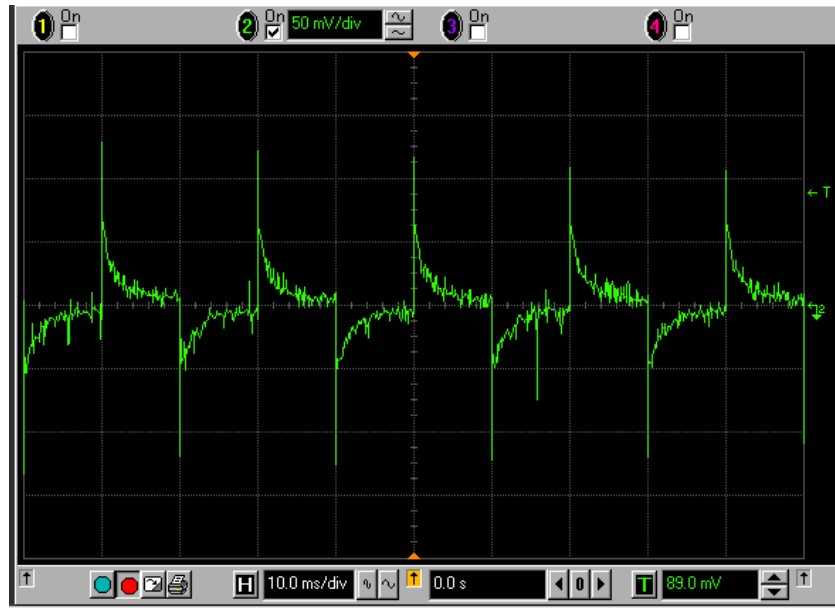


Figure 15. Load step where V_{out} is banded from 0.1 A to 2.5 A with a 1.0 A/ μ s slew-rate ($V_{in} = 230$ Vac).

Figures 14 and 15 represent the step load response from the standby mode to the wake-up mode, featuring a variation from 100 mA up to 2.5 A. The spike you can see

on the waveforms comes from the current discontinuity induced by the LC filter inductor L_1 .

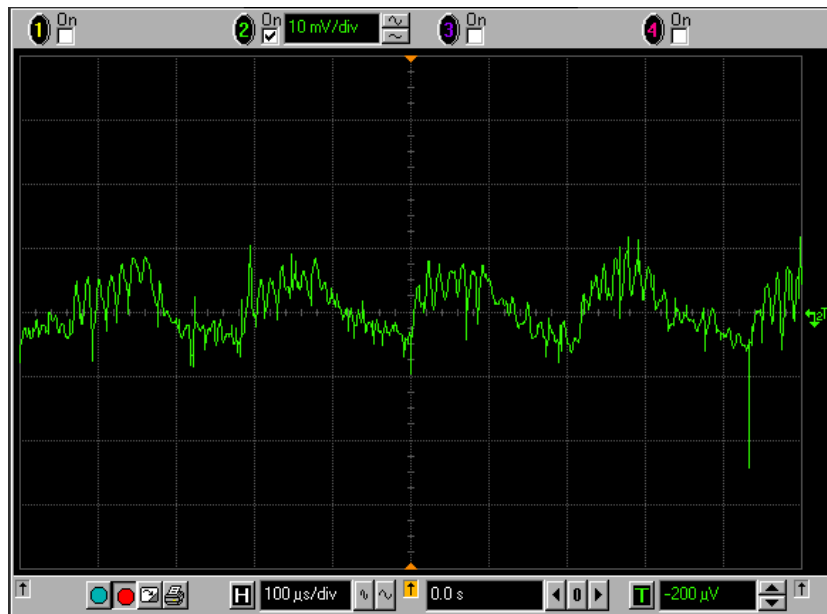


Figure 16. Peak-to-peak ripple, $P_{out} = 0.5$ W, Cable length = 30 cm, $V_{in} = 85$ Vac.

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Figure 17. Peak-to-peak ripple, $P_{out} = 0.5\text{ W}$, Cable length = 30 cm, $V_{in} = 230\text{ Vac}$.

Figures 16 and 17 display the ripple amplitude when the board enters skip cycle, mainly at a 0.5 W output power. The

measurement has been carried at two line levels and using 30 cm long cables to mimic a real PSU cabling connector.

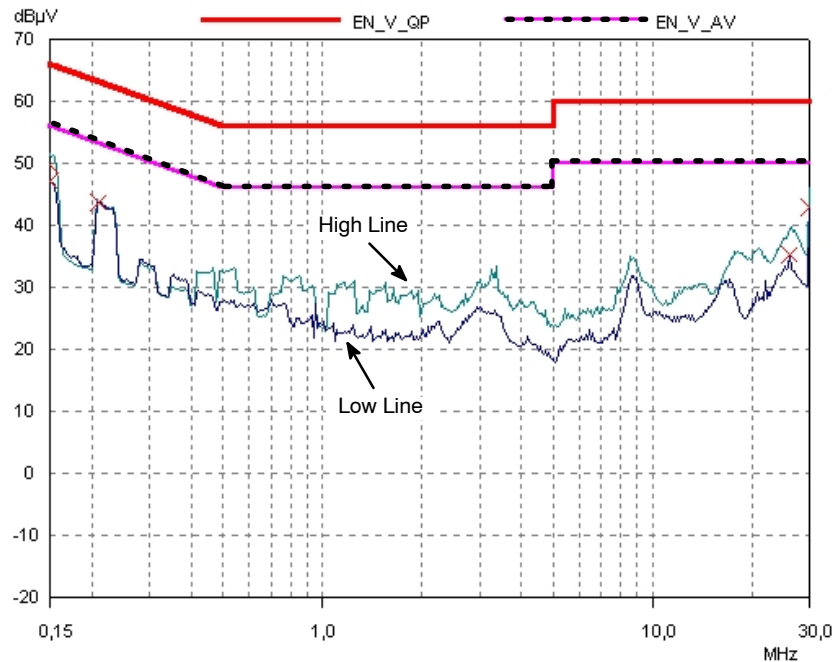


Figure 18. EMI signature, low line and high line in quasi-peak, $P_{out} = 10\text{ W}$.

Figure 18 shows the advantage of EMI jittering, offering a clean signature at both line levels. As the sweep is

successfully made in Quasi-Peak (QP) it implies immediate compliance in average mode.

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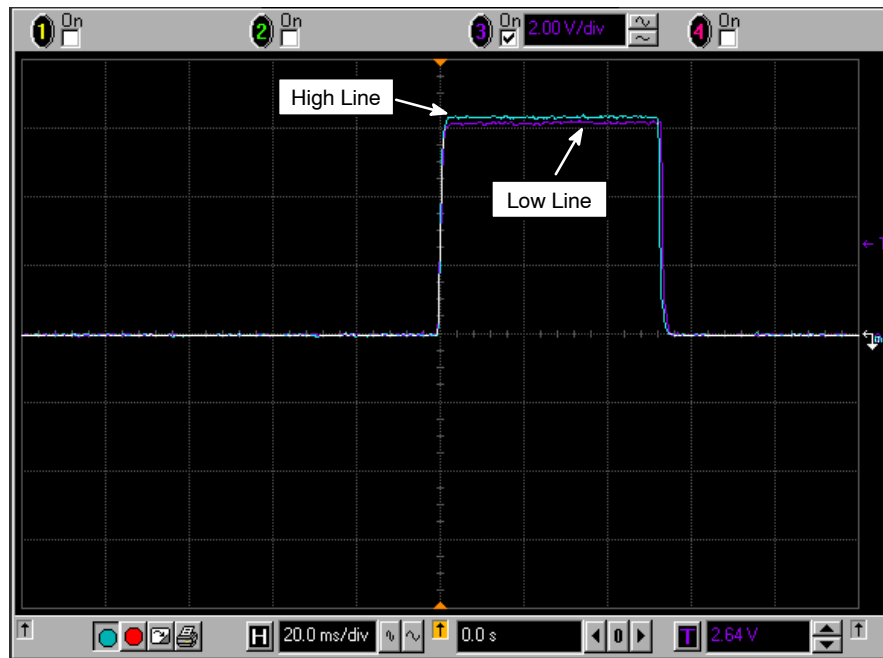


Figure 19. Peak Output Current in Short-Circuit at Both Line Conditions: 6.3 A

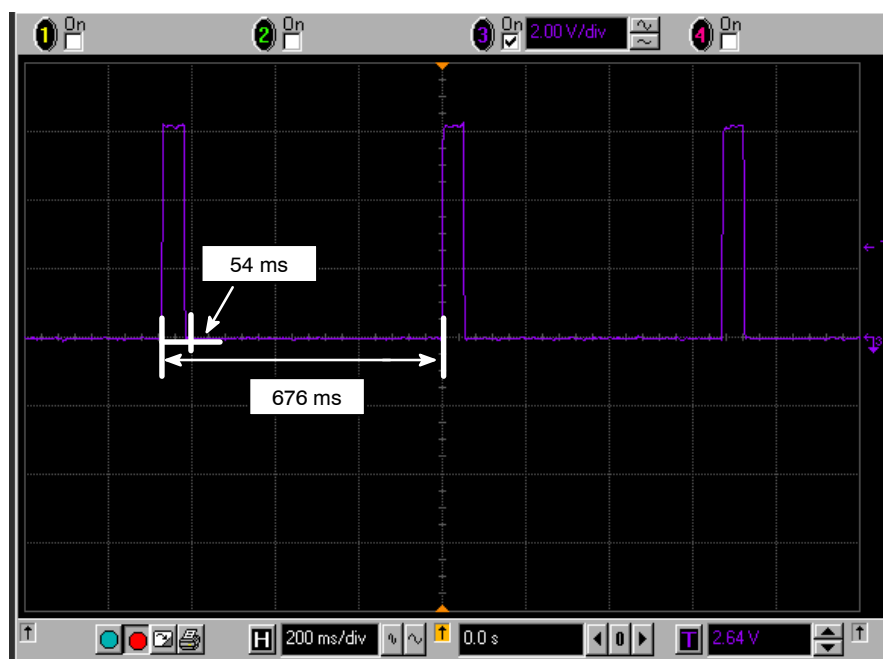


Figure 20. Output Current Waveform in Short-Circuit

Some PC application specs require the output average and RMS currents in short-circuit to stay within given limits. With this design, we have obtained the following results at high-line:

- $I_{\text{peak}} = 6.4 \text{ A}$
- $I_{\text{out,av}} = 6.4 \times 54 / 676 = 511 \text{ mA}$
- $I_{\text{out,rms}} = 6.4 \sqrt{\frac{54}{676}} = 1.8 \text{ A}$

PCB Views

The PCB routing includes large copper areas around the integrated circuit to maximize its power dissipation. The

diode is placed on the copper side and due to its low V_F it leads to good thermal performance.

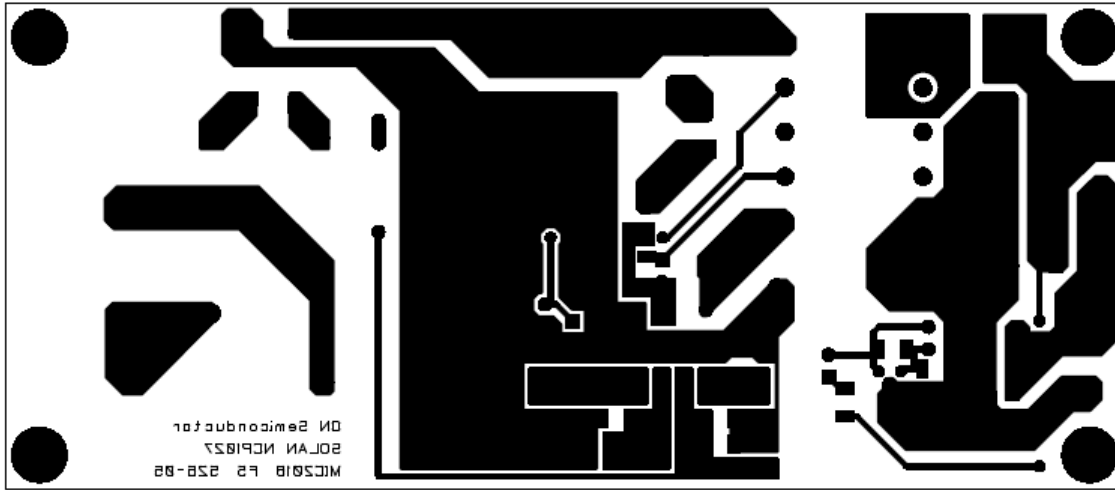


Figure 21. The PCB Copper Area of the Demonstration Board

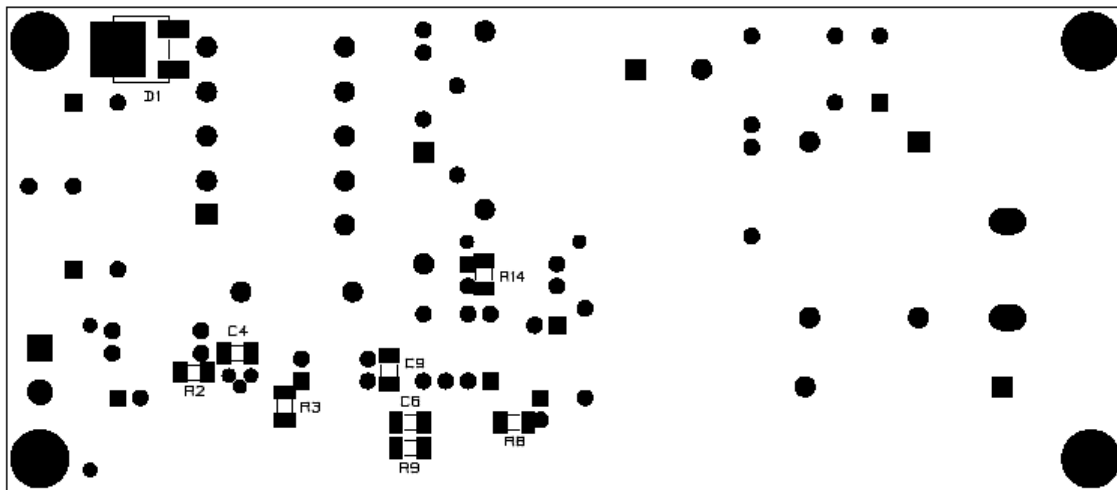


Figure 22. The SMD Positions on the Copper Side

NCP1027ATXGEVB

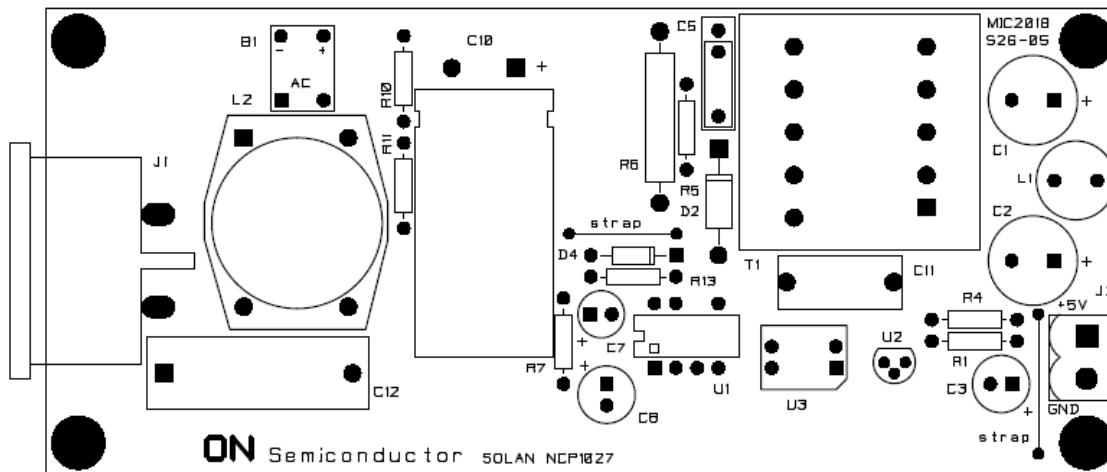


Figure 23. Component Side View

BILL OF MATERIAL

Table 1. BILL OF MATERIAL

Designator	QTY	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	RoHS Compliant
U1	1	High Voltage Switcher	NA	NA	PDIP 8	ON Semiconductor	NCP1027P065G	No	Yes
U2	1	Adjustable Shunt Regulator	2.5 V - 36 V, 1 mA - 100 mA	2%	TO-92	ON Semiconductor	TL431CLPRPG	No	Yes
U3	1	Optocoupler	70 V, 60 mA	NA	DIP-4	Vishay Semiconductors	SFH615A	No	Yes
B1	1	Single-Phase Bridge Rectifier	800 V, 1 A	NA	DFM	Vishay General	DF08ME3	Yes	Yes
C1, C2	2	Electrolytic Capacitor	1200 μ F, 16 V	20%	Radial	Panasonic	EEU-FC1C122	Yes	Yes
C10	1	Electrolytic Capacitor	47 μ F, 400 V	20%	Radial	Panasonic	ECA2GHG470	Yes	Yes
C11	1	Ceramic ac Capacitor, Class Y1	2.2 nF, 500 Vac, 50 Hz	20%	Leaded spacing = 12.5 mm	Vishay Draloric	WKP222MCPR	No	Yes
C12	1	Capacitor, Class X2	220 nF, 275 Vac	20%	Leaded spacing = 15 mm	Evov Rifa	PHE840MX6220M	No	Yes
C13	1	Electrolytic Capacitor	1 μ F, 50 V	20%	Radial	Panasonic	EEUFC1H1R0	Yes	Yes
C3	1	Electrolytic Capacitor	220 μ F, 16 V	20%	Radial	Panasonic	EEUFC1C221	Yes	Yes
C4	1	Multilayer Ceramic Capacitor, X7R	100 nF, 50 V	10%	1206	Epcos	B37872K5104K060	Yes	Yes
C5	1	Metallized Polyester Film Capacitor	10 nF, 630 V	10%	Lead spacing = 10 mm	Vishay Roederstein	MKT1822310635	Yes	Yes
C6	1	Multilayer Ceramic Capacitor, X7R	10 nF, 50 V	10%	1206	Epcos	B37872K5103K060	Yes	Yes
C7	1	Minature Aluminum Electrolytic Capacitor	10 μ F, 63 V	20%	Radial	Panasonic	ECA1JM100	Yes	Yes

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Table 1. BILL OF MATERIAL

Designator	QTY	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	RoHS Compliant
C8	1	Electrolytic Capacitor	100 μ F, 10 V	20%	Radial	Panasonic	EEUFC1A101	Yes	Yes
C9	1	Multilayer Ceramic Capacitor, X7R	1nF, 50 V	10%	1206	Epcos	B37872K5102K060	Yes	Yes
D1	1	Schottky Barrier Rectifier	35 V, 8 A	NA	DPAK-4	ON Semiconductor	MBRD835LG	No	Yes
D2, D4	2	Fast-Recovery Rectifier	600 V, 1 A	NA	Axial	ON Semiconductor	1N4937G	No	Yes
H1	1	PCB Connector	NA	NA	NA	Multicomp	JR-201S	Yes	Yes
H2	1	PCB Connector	NA	NA	NA	Weidmuller	1760510000	Yes	Yes
L1	1	Inductor	2.2 μ H, 6 A	20%	7.8 mm x 9.5 mm	Wurth Elektronik	744772022	Yes	Yes
L2	1	Common Mode Inductor	27 mH, 0.8 A	NA	22.5 mm x 21.5 mm	Schaffner	RN114-0.8/02	Yes	Yes
R1	1	Axial Lead Carbon Film Resistor	10 k Ω , 1/4 W	5%	Axial	Panasonic	ERD-S2TJ103V	Yes	Yes
R10	1	Metal Film Resistor	2.8 M Ω , 1/4 W	5%	Axial	Vishay Dale	CCF072M80JKE36	Yes	Yes
R11	1	Axial Lead Carbon Film Resistor	2.2 M Ω , 1/4 W	5%	Axial	Panasonic	ERD-S2TJ225V	Yes	Yes
R13	1	Axial Lead Carbon Film Resistor	47 k Ω , 1/4 W	5%	Axial	Panasonic	ERD-S2TJ473V	Yes	Yes
R14	1	Axial Lead Carbon Film Resistor	560 k Ω , 1/4 W	5%	Axial	Panasonic	ERD-S2TJ564V	Yes	Yes
R2	1	SMD Resistor	10 k Ω , 1/4 W	5%	1206	Vishay Dale	CRCW120610K0JNEA	Yes	Yes
R3	1	SMD Resistor	100 Ω , 1/4 W	5%	1206	Vishay Dale	CRCW1206100RJNEA	Yes	Yes
R4	1	Axial Lead Carbon Film Resistor	680 Ω , 1/4 W	5%	Axial	Panasonic	ERD-S2TJ681V	Yes	Yes
R5	1	Axial Lead Carbon Film Resistor	47 Ω , 1/4 W	5%	Axial	Panasonic	ERD-S2TJ470V	Yes	Yes
R6	1	Power Metal Film Resistor	150 k Ω , 1 W	5%	Axial	Vishay BC Components	PR01000201503JAC00	Yes	Yes
R7	1	Axial Lead Carbon Film Resistor	1 k Ω , 1/4 W	5%	Axial	Panasonic	ERD-S2TJ102V	Yes	Yes
R8	1	SMD Resistor	78 k Ω , 1/4 W	5%	1206	Vishay Dale	CRCW120678KJNEA	Yes	Yes
R9	1	SMD Resistor	27 k Ω , 1/4 W	5%	1206	Vishay Dale	CRCW120627KJNEA	Yes	Yes
T1	1	Transformer	3.4 mH	NA	1.1" x 1.1" x 0.95"	Coilcraft	DA2077-AL	No	Yes

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TEST PROCEDURE

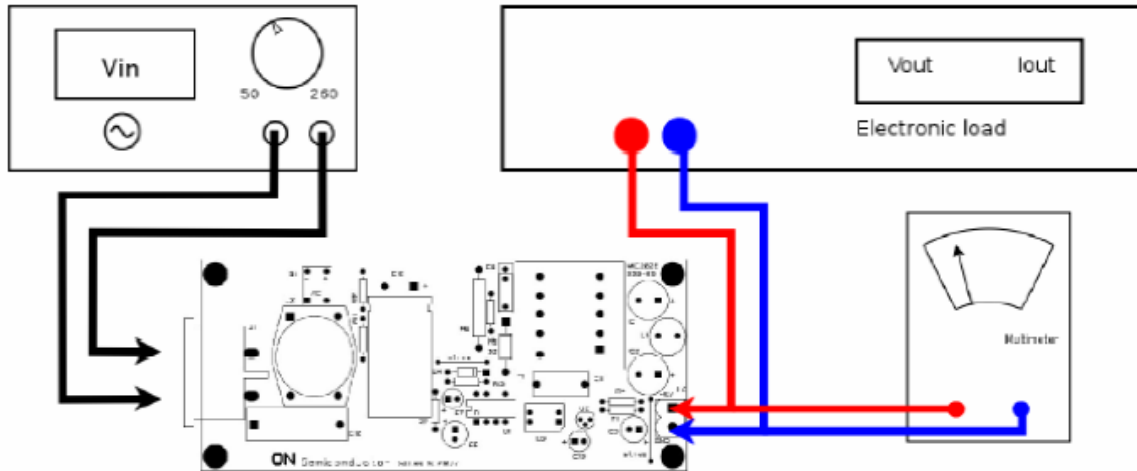


Figure 24. Test Setup

Required Equipment

- ac Power Supply, 85 Vac – 265 Vac, 1 A
- Electronic Load, 5 V up to 3 A
- Yokogawa Power Meter WT210
- NCP1027ATX Evaluation Board
- Multimeter


Test Procedure

1. Connect the test setup as shown in Figure 24.
2. Apply an input voltage, 85 Vac < VIN < 265 Vac, 50 Hz or 60 Hz.
3. Connect electronic load to output connector.
4. Test the conditions given in Table 2.

Table 2. DESIRED RESULTS

	Measurements	Conditions	Results	Comments
1	Output Voltage	V _{IN} = 100 Vac, no load	V _{OUT} = 5 V ± 5%	
2	Input consumption at high line and no load	V _{IN} = 230 Vac, no load	P _{IN} = 0.09 W ± 15%, V _{OUT} = 5 V	No load measurment can fluctuate, run WT210 in average mode
3	Input consumption at high line line and low load	V _{IN} = 230 Vac, I _{load} = 0.1 A	P _{IN} = 0.83 W ± 10% V _{OUT} = 5 V P _{OUT} = 0.5 W	
4	Output voltage at high line and full load	V _{IN} = 230 Vac, I _{load} = 2.5 A	V _{OUT} = 5 V ± 5%	
5	Output voltage at low line and full load	V _{IN} = 85 Vac, I _{load} = 2.5 A	V _{OUT} = 5 V ± 5%	
6	Brownout detection	V _{IN} ↓ until V _{OUT} = 0 V, I _{OUT} = 2 A	V _{IN} = 56 Vac ± 15%	Output voltage must collapse under 56 Vac
7	Maximum output at low line	V _{IN} = 85 Vac, I _{OUT} ↑	P _{OUTmax} = 14 W ± 15%	Output voltage must collapse above 14 W
8	Maximum output at high line	V _{IN} = 230 Vac, I _{OUT} ↑	P _{OUTmax} = 18 W ± 15%	Output voltage must collapse above 18 W

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